IPS Academy, Institute of Engineering & Science
(A UGC Autonomous Institute, Affiliated to RGPV, Bhopal)
Scheme & Syllabus Based on AICTE Flexible Curricula **(B. Tech)**
Electronics & Communication Engineering Department

Honors Degree Certification Course in VLSI Technology
(To be offered to students of ME, ECE departments)

S. No.	Subject Code	Semester	Subject Name	Contact Hours per week			Total Credits
				L	T	P	
1	HOMEEC-VT 101	I	Digital VLSI Design	2		2	3
2	HOMEEC- VT 201	II	IC Fabrication Technology	2	1	2	4
3	HOMEEC- VT 301	III	Digital System Design using HDL & PLDs	3	-	2	4
4	HOMEEC- VT 401	IV	Low Power VLSI Design	2	1	2	4
			Total	9	2	8	15

1 Hr Lecture	1 Hr Tutorial	2 Hr Practical
1 Credit	1 Credit	1 Credit

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HOMEEC-VT 101	**Digital VLSI Design**	**2L: 1T: 2P (05hrs)**	**Credits:04**

Recommended Prerequisite: Electronic Devices, Electronic Circuits, Digital circuits

Course Objective: In the course we provide a solid framework in understanding: Scaling of technology and their impact on interconnects, Interconnects as design objects, Noise in digital systems and its impact on system operation, Power distribution schemes for low noise, Signal and signalling conventions for on-chip and off-chip communication, Timing and synchronisation for fundamental operations and signalling & design rules.

MODULE 1 **(08 hrs)**
Introduction to MOSFETs : MOS Transistor Theory – Introduction MOS Device, Fabrication and Modeling , Body Effect, Noise Margin, Latch-up

MODULE 2 **(08 hrs)**
MOS Inverter : MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, Design Equations, Static Load MOS Inverters, Transistor Sizing, Static and Switching Characteristics; MOS Capacitor; Resistivity of Various Layers.

MODULE 3 **(08 hrs)**
Symbolic and Physical Layout Systems – MOS Layers Stick/Layout Diagrams; Layout Design Rules, Issues of Scaling, Scaling factor for device parameters.

MODULE 4 **(08 hrs)**
Combinational MOS Logic Circuits: Pass Transistors/Transmission Gates; Designing with transmission gates, Primitive Logic Gates; Complex Logic Circuits.

Sequential MOS Logic Circuits: SR Latch, clocked Latch and flip flop circuits, CMOS D latch and edge triggered flip flop.

MODULE 5 **(08 hrs)**
Dynamic Logic Circuits; Basic principle, non ideal effects, domino CMOS Logic, high performance dynamic CMOS Circuits, Clocking Issues, Two phase clocking. CMOS Subsystem Design: Semiconductor memories, memory chip organization, RAM Cells, dynamic memory cellSymbolic and Physical Layout Systems – MOS Layers Stick/Layout Diagrams; Layout Design

Assessment: Mid-term test, Assignment, Tutorial, Quiz and End semester exam.

List of Experiments:

1. Introduction to EDA Tool (LTSPICE/Microwind/Xillinx/FPGA Kit).
2. Design, Simulate & analysis of CMOS inverter transient & DC characteristics.
3. Design, Simulate & analysis of 2 input NAND gate using CMOS.
4 Design, Simulate & analysis of 2 input NOR gate using CMOS.
5. Design, Simulate & analysis of 2:1 MUX using pass transistor.
6. Design, Simulate & analysis CMOS logic for Half Adder/ Full Adder using CMOS. .
7. Study of the switching characteristics of CMOS Inverter and find out noise margins.
8. Design, Simulate & analysis of MOS Inverter with Pseudo NMOS Inverter.
9. Design, Simulate & analysis of MOS Inverter with Dynamic Logic Circuits
10. Design, Simulate & analysis of MOS Inverter with Capacitive Load

Assessment: Internal viva, Continuous evolution of experiments, Journal write-up, Quiz and End semester exam.

Course Outcomes:
Students earning credits will develop ability to:

1. Understand the Scaling of technology and their impact, MOSFET & Their parameters
2. Understand the reason of Propagation Delays & Calculation in MOS
3. Illustrate and Design and analyze of different type of logic gates with different loads.
4. Illustrate and Analyze of static & dynamic power in MOS Devices.
5. Understand the layout & stick diagram design rules.

Text/Reference Books:

REFERENCE BOOKS:

1. S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits : Analysis and Design, Third Edition,
MH, 2002.
2. W. Wolf, Modern VLSI Design : System on Chip, Third Edition, PH/Pearson, 2002.
3. N. Weste, K. Eshraghian and M. J. S. Smith, Principles of CMOS VLSI Design : A Systems
Perspective, Second Edition (Expanded), AW/Pearson, 2001.
4. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, Digital Integrated Circuits : A Design Perspective,
Second Edition, PH/Pearson, 2003.
5. D. A. Pucknell and K. Eshraghian, Basic VLSI Design : Systems and Circuits, Third Edition, PHI,
1994.
6. J. P. Uyemura, CMOS Logic Circuit Design, Kluwer, 1999.
7. J. P. Uyemura, Introduction to VLSI Circuits and System, Wiley, 2002.
8. R. J. Baker, H. W. Li and D. E. Boyce, CMOS Circuit Design, Layout and Simulation, PH, 1997.

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HOMEEC- VT 201	IC Fabrication Technology	2L: 1T: 2P (05 hrs)	Credits:04

Recommended Prerequisite: Electronic Devices, VLSI Basics, Digital circuits

Course Objective: The course is designed to give the student an understanding of the different design steps required to carry out a complete digital VLSI (Very-Large-Scale Integration) design in silicon and the fundamental concepts and structures of designing digital VLSI systems include CMOS devices and circuits, standard CMOS fabrication processes

MODULE 1 **(09 hrs)**
Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.
Impurity incorporation: Solid State diffusion modelling and technology; Ion Implantation modelling, technology and damage annealing; characterisation of Impurity profiles.

MODULE 2 **(07 hrs)**
Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterisation of oxide films; High k and low k dielectrics for ULSI.

MODULE 3 **(07 hrs)**
Lithography Process: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation

MODULE 4 **(08 hrs)**
Chemical Vapour Deposition Techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modelling and technology. **Metal film deposition :** Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallisation schemes.

MODULE 5 **(07 hrs)**
Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology.

Assessment: Mid-term test, Assignment, Tutorial, Quiz and End semester exam.

List of Experiments:

1. Study of micron-based & lambda based layout design rules.
2. Design, simulate & analysis layout of CMOS Inverter.
3. Design, simulate & analysis layout of 2 input NAND gate Inverter.
4. Design, simulate & analysis layout of 2 input NOR gate Inverter.
5. Design, simulate & analysis layout of pseudo NMOS.
6. Design, simulate & analysis layout of domino CMOS.
7. Design, simulate & analysis layout of dynamic CMOS.
8. Design, simulate & analysis layout of pass transistor logic.
9. Design, simulate & analysis layout of capacitive load.

10. Design, simulate & analysis layout of Half Adder.

Assessment: Internal viva, Continuous evolution of experiments, Journal write-up, Quiz and End semester exam.

Course Outcomes:

Students earning credits will develop ability to:

1. Understand the Basic fabrication steps for BJT & MOS with crystal growth.
2. Illustrate the various methods of Oxidation & diffusion used in fabrication.
3. Understand the methods of lithography & etching.
4. Illustrate the various methods of metallization, isolation & packaging.
5. Understand the various technology used in CMOS design.

Text /Reference Books:

1. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1994(2nd Edition).
2. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988.
3. Plummer, Deal , Griffin “Silicon VLSI Technology: Fundamentals, Practice & Modeling” PH, 2001.
4. P. VanZant , “Microchip Fabrication”, 5th Edition, MH , 200

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HOMEEC- VT 301	**HDL & PLDs**	**2L: 1T: 2P (05 hrs.)**	**Credits: 03**

Recommended Prerequisite: Electronic Devices, VLSI Basics, Digital circuits

Course Objective: The course is designed to give the student an understanding of the different design steps required to carry out a complete digital VLSI (Very-Large-Scale Integration) design in silicon and the fundamental concepts and structures of designing digital VLSI systems include Synchronous Sequential Circuits, VHDL programming, PLds & memory devices.

MODULE I **(8 hrs.)**
Sequential Circuit Design: Design of Synchronous Sequential Circuits, Mealy & Moore Circuits, Analysis of Synchronous Sequential Circuits, Top-down Design, Controller Design, Control algorithm and State diagram.

MODULE II **(8 hrs.)**
VHDL Programming: Entity, Architecture and Operators, Concurrency, Data flow and Behavioural models, Structural Model, Simulation, Simulating Concurrency, Classes and Data types, Concurrent statements and Sequential statements, Sequential statements and Loops, Modelling flip-flops, Registers, Synthesis of Sequential circuits, Libraries and Packages, Operators, Delay modeling, Delay modeling, VHDL Examples, FSM Clock, VHDL coding of FSM, Synchronization.

MODULE III **(9 hrs.)**
Programmable Logic Devices: Evolution of PLDs, Simple PLDs: Fitting, Complex PLDs, FPGA Introduction, FPGA Interconnection, Design Methodology, Xilinx Virtex FPGA's CLB, Xilinx Virtex Resource Mapping, IO Block, Xilinx Virtex Clock Tree, FPGA Configuration, Altera and Actel FPGAs, VHDL Test bench, Case study on FPGA Board

MODULE IV **(8 hrs.)**
Semiconductor Memories: Memory Classification, Memory Architectures and Building Blocks, Introduction to Static and Dynamic RAMs, **Static Random Access Memory (SRAM),** SRAM Basics, CMOS SRAM Cell CMOS SRAM Cell Design, READ Operation, WRITE Operation, DRAM Basics, Differential Operation In Dynamic RAMs, DRAM Read Process With Dummy Cell, Operation Of The Read Circuit, Calculation Of Change In Bit line Voltage, Area Considerations, Metal Gate Diffusion Storage

MODULE V **(7 hrs.)**
SRAM and DRAM Peripherals: SRAM and its Peripherals, DRAM and its Peripherals, Semiconductor Read Only Memory (ROM), NOR based ROM Array, NAND based ROM Array. **Few special Memories:** Non-Volatile READ-WRITE Memory, The Floating Gate Transistor Erasable Programmable Read Only Memory (EPROM), Electrically Erasable Programmable Read Only Memory (E2PROM)

Assessment: Internal viva, Continuous evolution of experiments, Journal write-up, Quiz and End semester exam.

Course outcome:

Students earning credits will develop ability to:

1. Explain & analyze the basic design of synchronous sequential circuits.
2. Learn the VHDL programming for various CMOS circuits.
3. Illustrate the different type of PLDs & FPGA.
4. Design various types of memory devices like SRAM Basics, CMOS SRAM Cell CMOS SRAM Cell Design
5. Design the different type of SRAM and DRAM Peripherals.

Experiments List:

1. Introduction to VLSI lab (Xilinx, ISE Microwind tool, VHDL Verilog code)
2. Design of logic Gates: AND, OR, NOT, NAND, NOR, XOR, XNOR.
3. Design of Half-Adder, Full Adder, Half Subtractor, Full Subtractor.
4. Design of 8:1 MUX.
5. Design of 3 : 8 Decoder.
6. Design of 1:8Dmux.
7. Design of binary to gray code converter.
8. Design of all type of Flip-Flops using (if-then-else) Sequential Constructs
9. Simulate 1-bit full adder following behavioral and structural modeling using VHDL\Verilog. 11. Implement all the logic gates in FPGA using verilog HDL. (Xilinx/ FPGA Kit).
10. Implement using 1-bit half adder and1-bit Full adder in FPGA using verilog HDL (Xilinx/ FPGA Kit).

Text/References Books:

1. Digital Logic Design and Computer Organization: With Computer Architecture for Security, Nikrouz Faroughi, and Publication Date &Copyright: 2015 McGraw-Hill Education.
2. Disciplines in Combinational and Sequential Circuit Design (Electrical & Electronic Engineering S.) Hardcover – 1 August 1970 **by** R.M.M. Oberman (Author)
3. VHDL: Programming by Example Hardcover – Import, 16 July 200 **by** Douglas Perry (Author)
4. P. J. Ashenden, "The Designer's Guide to VHDL"
5. Practical Programmable Circuits: A Guide to PLDs, State Machines, and Microcontrollers Kindle Editionby James D. Broesch (Author) Format: Kindle Edition
6. Programmable Logic Handbook: PLDs, CPLDs and FPGAs (McGraw-Hill Handbooks) 16 May 1998by Ashok Sharma (Author)
7. VLSI Memory Chip Design Paperback – 1 January 2006 by Kiyoo Itoh (Author)
8. VLSI Memory Chip Design (Springer Series in Advanced Microelectronics, 5) 1st ed. 2001 Edition by Kiyoo Itoh (Author)

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HOVTEC- VT 401	**Low Power VLSI Design**	**3L: 0T: 0P (03 hrs.)**	**Credits: 03**

Prerequisite: Electronic Devices, VLSI Basics, Digital circuits

Course Objective: The course is designed to give the student an understanding of the different design steps required to carry out a complete digital VLSI (Very-Large-Scale Integration) design in silicon and the fundamental concepts and structures of designing digital VLSI systems include device modeling & circuit simulation, power dissipation, Supply Voltage Scaling Approaches**,** Leakage Power minimization Approaches.

MODULE I **(8 hrs.)**
Device Modeling & Circuit Simulation: Dc Models, Small Signal Models, MOS Models, MOSFET Models in High Frequency and small signal, Short channel devices, Sub threshold Operations, Modeling Noise Sources in MOSFET's, **Circuit Simulation:** Introduction, Circuit Simulation Using Spice, MOSFET Model, Level 1 Large signal model, Level 2 Large Signal Model, High Frequency Model, Noise Model of MOSFET,

MODULE II **(8 hrs.)**
Sources of Power dissipation: Dynamic Power Dissipation Short Circuit Power Switching Power Gliching Power Static Power Dissipation Degrees of Freedom

MODULE III **(8 hrs.)**
Supply Voltage Scaling Approaches: Device feature size scaling Multi-Vdd Circuits Architectural level approaches: Parallelism, Pipelining Voltage scaling using high-level transformations Dynamic voltage scaling Power Management =

MODULE IV **(9 hrs.)**
Switched Capacitance Minimization Approaches: Hardware Software Tradeoff Bus Encoding Two's complement Vs Sign Magnitude Architectural optimization Clock Gating Logic styles

MODULE V **(7 hrs.)**
Leakage Power minimization Approaches: Variable-threshold-voltage CMOS (VTCMOS) approach Multi-threshold-voltage CMOS (MTCMOS) approach Power gating Transistor stacking Dual-Vt assignment approach (DTCMOS) Adiabatic Switching Circuits Battery-aware Synthesis Variation tolerant design CAD tools for low power synthesis.

Assessment: Internal viva, Continuous evolution of experiments, Journal write-up, Quiz and End semester exam.

Course outcome:

Students earning credits will develop ability to:

1. Student will able to learn device modeling & circuit simulation.
2. The students will be able to understand the sources of power dissipation.
3. The students will be able to understand the Supply Voltage Scaling Approaches
4. The students will be able to understand the Switched Capacitance Minimization Approaches & different techniques.
5. The students will be able to understand the Leakage Power minimization Approaches & their applications.

List of experiments:

1. Design & simulate Low power Adders
2. Design & simulate Power delay measurement of Adders
3. Design & simulate Low power Multipliers
4. Design & simulate Power delay measurement of Multipliers.
5. Design & simulate Leakage current analysis and reduction techniques for low power VLSI circuits.
6. Design & simulate Power distribution of wireless ad-hoc network with topology control.
7. Design & simulate Noise tolerance enhancement techniques for low power and high performance VLSI circuits.
8. Design & simulate An efficient energy saving mechanism for IEEE 802.16e wireless MAN.
9. Performance evaluation of Deep Submicron Logic Circuits for low voltage, low power and high speed VLSI applications.
10. Analysis and designing of low leakage SRAM cells

Text/References Books:

1. Sung Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata Mcgrag Hill.
2. Neil H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design, 2nd Edition, Addison Wesley (Indian reprint).
3. A. Bellamour, and M. I. Elmasri, Low Power VLSI CMOS Circuit Design, Kluwer Academic Press, 1995.
4. Anantha P. Chandrakasan and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers, 1995.
5. Kaushik Roy and Sharat C. Prasad, Low-Power CMOS VLSI Design, Wiley-Inter science, 2000.
6. Jan Rabaey, “Low Power Design Essentials”, Springer Publications.
7. Chandrakasan and R. Brodersen, “Low-Power CMOS Design”, IEEE Press.
8. Gary Yeap, “Practical Low Power Digital VLSI Design”, Springer Publications.