IPS Academy, Institute of Engineering & Science
(A UGC Autonomous Institute, Affiliated to RGPV, Bhopal)
Scheme & Syllabus Based on AICTE Flexible Curricula **(B. Tech)**
Electronics & Communication Engineering Department

Honors Degree Certification Course in VLSI Design & Technology
(To be offered to students of ECE departments)

S. No.	Subject Code	Category	Semester	Subject Name	Contact Hours per week			Total Credits
					L	T	P	
1			V	VLSI Design Basics	2		2	3
2			VI	CMOS Fabrication Technology	2	1	2	4
3			VII	Digital System Design using HDL & PLDs	3	-	2	4
4			VIII	Low Power VLSI Design	2	1	2	4
				Total	9	2	8	15

1 Hr Lecture	1 Hr Tutorial	2 Hr Practical
1 Credit	1 Credit	1 Credit

Note: *VII semester subject (Digital System Design using HDL & PLDs or any other course equivalent to Digital System Design using HDL & PLDs) can also be done from MOOC courses (NPTEL, SWAYAM, EDx etc.).

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	VLSI Design Basics	**2L: 1T: 2P (05hrs)**	**Credits:04**

Recommended Prerequisite: Electronic Devices, Electronic Circuits, Digital circuits

Course Objective: In the course we provide a solid framework in understanding: Scaling of technology and their impact on interconnects, Interconnects as design objects, Noise in digital systems and its impact on system operation, Power distribution schemes for low noise, Signal and signalling conventions for on-chip and off-chip communication, Timing and synchronisation for fundamental operations and signalling & design rules.

MODULE 1 **(08 hrs)**
System approach to VLSI Design: Introduction to MOSFET, MOSFET I-V Modelling, MOS Capacitor, Modes of operation, MOSFET I-V characteristics, Types of Scaling , Short channel effect , Velocity saturation , Short Channel Effects, Mobility degradation, Subthreshold current, Threshold voltage variation, Drain induced barrier lowering (DIBL) , Drain punch through, Hot carrier effect , Surface states and interface trapped charge

MODULE 2 **(08 hrs)**
Propagation Delays & Calculation in MOS: CMOS Inverter Characteristics, Noise Margins, Regions of operation, Beta-n by Beta-p ratio, Propagation Delay Calculation of CMOS Inverter, Quick Estimates, Rise and Fall times Calculation, Logical Effort, Delay in a Logical Gate, Logical Effort of an Inverter, NAND Gate, NOR Gate & XOR Gate, Logic Effort Calculation of few Mixed Circuits, Delay Plot, Logical Effort of Multistage Logic Networks, Minimizing Delay along a Path.

MODULE 3 **(08 hrs)**
Designing Asymmetric Logic Gates: Application of Asymmetric Logic Gates, Analyzing Delays, Pseudo NMOS, Circuits Different Configurations with NMOS Inverter, Pseudo NMOS Inverter, Calculation of Capacitive Load, Design Techniques for large Fan-in, Ratioed Logic, Pass Transistor Logic, Dynamic Logic Circuits, Negative D-Latch, S-R Latch using NOR Gates, Simple Latch using two Inverters (Bistable Element),Master Slave Flip-Flop.

MODULE 4 **(08 hrs)**
Power Dissipation in CMOS Circuits Effect of Power Dissipation, How to Reduce Temperature, Components of Power Dissipation, Static Power Dissipation, Dynamic Power Dissipation, Methods to Reduce Power Dissipation Short-Circuit Power Dissipation

MODULE 5 **(08 hrs)**
Layout Design Rules: Layout Design Rules, Types of Design Rules, Layer Representations, Stick Diagrams, λ-based Design Rules, MOS Combinational Circuits - Different Logic diagram

Assessment: Mid-term test, Assignment, Tutorial, Quiz and End semester exam.

List of Experiments:

1. Introduction to EDA Tool (LTSPICE/Microwind/Xillinx/FPGA Kit).
2. Design, Simulate & analysis of CMOS inverter transient & DC characteristics.
3. Design, Simulate & analysis of 2 input NAND gate using CMOS.
4 Design, Simulate & analysis of 2 input NOR gate using CMOS.

5. Design, Simulate & analysis of 2:1 MUX using pass transistor.
6. Design, Simulate & analysis CMOS logic for Half Adder/ Full Adder using CMOS. .
7. Study of the switching characteristics of CMOS Inverter and find out noise margins.
8. Design, Simulate & analysis of MOS Inverter with Pseudo NMOS Inverter.
9. Design, Simulate & analysis of MOS Inverter with Dynamic Logic Circuits
10. Design, Simulate & analysis of MOS Inverter with Capacitive Load

Assessment: Internal viva, Continuous evolution of experiments, Journal write-up, Quiz and End semester exam.

Course Outcomes:
Students earning credits will develop ability to:

1. Understand the Scaling of technology and their impact, MOSFET & Their parameters
2. Understand the reason of Propagation Delays & Calculation in MOS
3. Illustrate and Design and analyze of different type of logic gates with different loads.
4. Illustrate and Analyze of static & dynamic power in MOS Devices.
5. Understand the layout & stick diagram design rules.

Text/Reference Books:

1. Geiger, Allen and Strader, "VLSI Design Techniques for Analog and Digital Circuits", International Edition, TMH Publication, 1990.
2. Sorab Gandhi, "VLSI Fabrication Principles", 2nd Edition, Wiley-Interscience Publication, 1994.
3. Weste and Eshraghian, "Principles of CMOS VLSI design", 2nd Edition, Pearson Education, 1993.
4. Weste, Harris and Banerjee, "CMOS VLSI Design", 3rd Edition, Pearson Education, 2007.
5. Pucknell and Eshraghian, "Basic VLSI Design", 3rd Edition, PHI Learning, 1995.
6. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation" 2nd Edition, Wiley India, 2011.
7. S. M. Sze, "VLSI Technology", 2nd Edition, TMH Publication, 2017.

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	VLSI Technology	**2L: 1T: 2P (05 hrs)**	**Credits:04**

Recommended Prerequisite: Electronic Devices, VLSI Basics, Digital circuits

Course Objective: The course is designed to give the student an understanding of the different design steps required to carry out a complete digital VLSI (Very-Large-Scale Integration) design in silicon and the fundamental concepts and structures of designing digital VLSI systems include CMOS devices and circuits, standard CMOS fabrication processes

MODULE 1 **(09 hrs)**
Introduction on VLSI Design: Bipolar Junction Transistor Fabrication, MOSFET Fabrication for IC, Crystal Structure of Si, Defects in Crystal + Crystal growth, Epitaxy, Vapor phase Epitaxy, Doping during Epitaxy, Molecular beam Epitaxy

MODULE 2 **(8 hrs)**
Oxidation: Kinetics of Oxidation, Oxidation rate constants, Dopant Redistribution, Oxidation IV - Oxide Charges,
Diffusion: Theory of Diffusion, Infinite Source, Actual Doping Profiles, Diffusion IV Diffusion Systems, Ion - Implantation

MODULE 3 **(07 hrs)**
Lithography Process: Annealing of Damages, Masking during Implantation, Lithography, Wet Chemical Etching, Dry Etching, Plasma Etching Systems, Etching of Si, Sio2, SiN and other materials, Plasma Deposition Process, Metallization, Problems in Aluminium Metal contacts.

MODULE 4 **(08 hrs)**
IC BJT from junction isolation to LOCOS, Problems in LOCOS + Trench isolation, More about BJT Fabrication and Realization, Circuits + Transistors in ECL Circuits, MOSFET I - Metal gate vs. Self-aligned Poly-gate, MOSFET II Tailoring of Device Parameters, packaging, testing.

MODULE 5 **(07 hrs)**
CMOS Technology: A Basic n-well CMOS Process, Twin Tub Processes, CMOS Process Enhancement, Interconnects and Circuit Elements, Layout Design Rules, Latch up, Physical Origin, Latchup Triggering, Internal Latch up Prevention Techniques, Latch - up in CMOS, BICMOS Technology, planar CMOS technology & non-planar CMOS technology.

Assessment: Mid-term test, Assignment, Tutorial, Quiz and End semester exam.

List of Experiments:

1. Study of micron-based & lambda based layout design rules.
2. Design, simulate & analysis layout of CMOS Inverter.
3. Design, simulate & analysis layout of 2 input NAND gate Inverter.
4. Design, simulate & analysis layout of 2 input NOR gate Inverter.
5. Design, simulate & analysis layout of pseudo NMOS.
6. Design, simulate & analysis layout of domino CMOS.
7. Design, simulate & analysis layout of dynamic CMOS.

8. Design, simulate & analysis layout of pass transistor logic.
9. Design, simulate & analysis layout of capacitive load.
10. Design, simulate & analysis layout of Half Adder.

Assessment: Internal viva, Continuous evolution of experiments, Journal write-up, Quiz and End semester exam.

Course Outcomes:

Students earning credits will develop ability to:

1. Understand the Basic fabrication steps for BJT & MOS with crystal growth.
2. Illustrate the various methods of Oxidation & diffusion used in fabrication.
3. Understand the methods of lithography & etching.
4. Illustrate the various methods of metallization, isolation & packaging.
5. Understand the various technology used in CMOS design.

Text /Reference Books:

1. Geiger, Allen and Strader, "VLSI Design Techniques for Analog and Digital Circuits", International Edition, TMH Publication, 1990.
2. Sorab Gandhi, "VLSI Fabrication Principles", 2nd Edition, Wiley-Interscience Publication, 1994.
3. Weste and Eshraghian, "Principles of CMOS VLSI design", 2nd Edition, Pearson Education, 1993.
4. Weste, Harris and Banerjee, "CMOS VLSI Design", 3rd Edition, Pearson Education, 2007.
5. Pucknell and Eshraghian, "Basic VLSI Design", 3rd Edition, PHI Learning, 1995.
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	Digital System Design using HDL & PLDs	**2L: 1T: 2P (05 hrs.)**	**Credits: 03**

Recommended Prerequisite: Electronic Devices, VLSI Basics, Digital circuits

Course Objective: The course is designed to give the student an understanding of the different design steps required to carry out a complete digital VLSI (Very-Large-Scale Integration) design in silicon and the fundamental concepts and structures of designing digital VLSI systems include Synchronous Sequential Circuits, VHDL programming, PLds & memory devices.

MODULE I **(8 hrs.)**
Sequential Circuit Design: Design of Synchronous Sequential Circuits, Mealy & Moore Circuits, Analysis of Synchronous Sequential Circuits, Top-down Design, Controller Design, Control algorithm and State diagram.

MODULE II **(8 hrs.)**
VHDL Programming: Entity, Architecture and Operators, Concurrency, Data flow and Behavioural models, Structural Model, Simulation, Simulating Concurrency, Classes and Data types, Concurrent statements and Sequential statements, Sequential statements and Loops, Modelling flip-flops, Registers, Synthesis of Sequential circuits, Libraries and Packages, Operators, Delay modeling, Delay modeling, VHDL Examples, FSM Clock, VHDL coding of FSM, Synchronization.

MODULE III **(9 hrs.)**
Programmable Logic Devices: Evolution of PLDs, Simple PLDs: Fitting, Complex PLDs, FPGA Introduction, FPGA Interconnection, Design Methodology, Xilinx Virtex FPGA's CLB, Xilinx Virtex Resource Mapping, IO Block, Xilinx Virtex Clock Tree, FPGA Configuration, Altera and Actel FPGAs, VHDL Test bench, Case study on FPGA Board

MODULE IV **(8 hrs.)**
Semiconductor Memories: Memory Classification, Memory Architectures and Building Blocks, Introduction to Static and Dynamic RAMs, **Static Random Access Memory (SRAM),** SRAM Basics, CMOS SRAM Cell CMOS SRAM Cell Design, READ Operation, WRITE Operation, DRAM Basics, Differential Operation In Dynamic RAMs, DRAM Read Process With Dummy Cell, Operation Of The Read Circuit, Calculation Of Change In Bit line Voltage, Area Considerations, Metal Gate Diffusion Storage

MODULE V **(7 hrs.)**
SRAM and DRAM Peripherals: SRAM and its Peripherals, DRAM and its Peripherals, Semiconductor Read Only Memory (ROM), NOR based ROM Array, NAND based ROM Array. **Few special Memories:** Non-Volatile READ-WRITE Memory, The Floating Gate Transistor Erasable Programmable Read Only Memory (EPROM), Electrically Erasable Programmable Read Only Memory (E2PROM)

Assessment: Internal viva, Continuous evolution of experiments, Journal write-up, Quiz and End semester exam.

Course outcome:

Students earning credits will develop ability to:

1. Explain & analyze the basic design of synchronous sequential circuits.
2. Learn the VHDL programming for various CMOS circuits.
3. Illustrate the different type of PLDs & FPGA.
4. Design various types of memory devices like SRAM Basics, CMOS SRAM Cell CMOS SRAM Cell Design
5. Design the different type of SRAM and DRAM Peripherals.

Experiments List:

1. Introduction to VLSI lab (Xilinx, ISE Microwind tool, VHDL Verilog code)
2. Design of logic Gates: AND, OR, NOT, NAND, NOR, XOR, XNOR.
3. Design of Half-Adder, Full Adder, Half Subtractor, Full Subtractor.
4. Design of 8:1 MUX.
5. Design of 3 : 8 Decoder.
6. Design of 1:8Dmux.
7. Design of binary to gray code converter.
8. Design of all type of Flip-Flops using (if-then-else) Sequential Constructs
9. Simulate 1-bit full adder following behavioral and structural modeling using VHDL\Verilog. 11. Implement all the logic gates in FPGA using verilog HDL. (Xilinx/ FPGA Kit).
10. Implement using 1-bit half adder and1-bit Full adder in FPGA using verilog HDL (Xilinx/ FPGA Kit).

Text/References Books:

1. Digital Logic Design and Computer Organization: With Computer Architecture for Security, Nikrouz Faroughi, and Publication Date &Copyright: 2015 McGraw-Hill Education.
2. Disciplines in Combinational and Sequential Circuit Design (Electrical & Electronic Engineering S.) Hardcover – 1 August 1970 **by** R.M.M. Oberman (Author)
3. VHDL: Programming by Example Hardcover – Import, 16 July 200 **by** Douglas Perry (Author)
4. P. J. Ashenden, "The Designer's Guide to VHDL"
5. Practical Programmable Circuits: A Guide to PLDs, State Machines, and Microcontrollers Kindle Editionby James D. Broesch (Author) Format: Kindle Edition
6. Programmable Logic Handbook: PLDs, CPLDs and FPGAs (McGraw-Hill Handbooks) 16 May 1998by Ashok Sharma (Author)
7. VLSI Memory Chip Design Paperback – 1 January 2006 by Kiyoo Itoh (Author)
8. VLSI Memory Chip Design (Springer Series in Advanced Microelectronics, 5) 1st ed. 2001 Edition by Kiyoo Itoh (Author)

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PEC-EC703 (C)	**Low Power VLSI Design**	**3L: 0T: 0P (03 hrs.)**	**Credits: 03**

Prerequisite: Electronic Devices, VLSI Basics, Digital circuits

Course Objective: The course is designed to give the student an understanding of the different design steps required to carry out a complete digital VLSI (Very-Large-Scale Integration) design in silicon and the fundamental concepts and structures of designing digital VLSI systems include device modeling & circuit simulation, power dissipation, Supply Voltage Scaling Approaches**,** Leakage Power minimization Approaches.

MODULE I **(8 hrs.)**
Device Modeling & Circuit Simulation: Dc Models, Small Signal Models, MOS Models, MOSFET Models in High Frequency and small signal, Short channel devices, Sub threshold Operations, Modeling Noise Sources in MOSFET's, **Circuit Simulation:** Introduction, Circuit Simulation Using Spice, MOSFET Model, Level 1 Large signal model, Level 2 Large Signal Model, High Frequency Model, Noise Model of MOSFET,

MODULE II **(8 hrs.)**
Sources of Power dissipation: Dynamic Power Dissipation Short Circuit Power Switching Power Gliching Power Static Power Dissipation Degrees of Freedom

MODULE III **(8 hrs.)**
Supply Voltage Scaling Approaches: Device feature size scaling Multi-Vdd Circuits Architectural level approaches: Parallelism, Pipelining Voltage scaling using high-level transformations Dynamic voltage scaling Power Management =

MODULE IV **(9 hrs.)**
Switched Capacitance Minimization Approaches: Hardware Software Tradeoff Bus Encoding Two's complement Vs Sign Magnitude Architectural optimization Clock Gating Logic styles

MODULE V **(7 hrs.)**
Leakage Power minimization Approaches: Variable-threshold-voltage CMOS (VTCMOS) approach Multi-threshold-voltage CMOS (MTCMOS) approach Power gating Transistor stacking Dual-Vt assignment approach (DTCMOS) Adiabatic Switching Circuits Battery-aware Synthesis Variation tolerant design CAD tools for low power synthesis.

Assessment: Internal viva, Continuous evolution of experiments, Journal write-up, Quiz and End semester exam.

Course outcome:

Students earning credits will develop ability to:

1. Student will able to learn device modeling & circuit simulation.
2. The students will be able to understand the sources of power dissipation.
3. The students will be able to understand the Supply Voltage Scaling Approaches
4. The students will be able to understand the Switched Capacitance Minimization Approaches & different techniques.
5. The students will be able to understand the Leakage Power minimization Approaches & their applications.

List of experiments:

1. Design & simulate Low power Adders
2. Design & simulate Power delay measurement of Adders
3. Design & simulate Low power Multipliers
4. Design & simulate Power delay measurement of Multipliers.
5. Design & simulate Leakage current analysis and reduction techniques for low power VLSI circuits.
6. Design & simulate Power distribution of wireless ad-hoc network with topology control.
7. Design & simulate Noise tolerance enhancement techniques for low power and high performance VLSI circuits.
8. Design & simulate An efficient energy saving mechanism for IEEE 802.16e wireless MAN.
9. Performance evaluation of Deep Submicron Logic Circuits for low voltage, low power and high speed VLSI applications.
10. Analysis and designing of low leakage SRAM cells

Text/References Books:

1. Sung Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata Mcgrag Hill.
2. Neil H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design, 2nd Edition, Addison Wesley (Indian reprint).
3. A. Bellamour, and M. I. Elmasri, Low Power VLSI CMOS Circuit Design, Kluwer Academic Press, 1995.
4. Anantha P. Chandrakasan and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers, 1995.
5. Kaushik Roy and Sharat C. Prasad, Low-Power CMOS VLSI Design, Wiley-Interscience, 2000.
6. Jan Rabaey, “Low Power Design Essentials”, Springer Publications.
7. Chandrakasan and R. Brodersen, “Low-Power CMOS Design”, IEEE Press.
8. Gary Yeap, “Practical Low Power Digital VLSI Design”, Springer Publications.